

Appl. No. 10/071,862
Amdt. Dated 08/03/2005
Reply to Office Action of 04/06/2005

IN THE CLAIMS

Please cancel claims 1-5 and 27-70 without prejudice.

Please amend claims 6, 9-12, 14-16, and 19-26 as follows below.

Please add new claims 71-90 as follows below.

MARKED-UP LISTING OF CLAIMS

1 1-5. (Cancelled)

1 6. (Currently Amended) A method of routing an

2 integrated circuit (IC) design, comprising:

3 accessing the IC design including a plurality of

4 objects having at least two metal routing ~~on one or more~~

5 layers;

6 accessing a first level for the IC design, wherein the

7 first level of the IC design is partitioned into a first

8 plurality of ~~one or more~~ partitions, and the plurality of

9 objects of the IC design are among the first plurality of

10 ~~one or more~~ partitions; and

11 forming a second level for the IC design, including:

12 partitioning the [[second]] first level of the IC

13 design into a second plurality of partitions, wherein

14 one or more partitions of the first plurality of

15 partitions is represented by at least two partitions of
16 the second plurality of partitions; and
17 within each partition of the second plurality of
18 partitions, interconnecting objects substantially
19 independently of other partitions of the second
20 plurality of partitions using the at least two metal
21 routing layers.

1 7. (Original) The method of claim 6, wherein
2 the routing is multithreaded at least at a first time.

1 8. (Original) The method of claim 6, wherein
2 the routing is single threaded at least at a first
3 time.

1 9. (Currently Amended) The method of claim 6, wherein
2 one or more partitions of the first plurality of ~~one or~~
3 ~~more~~ partitions has no objects of the plurality of objects.

1 10. (Currently Amended) The method of claim 6, wherein
2 every partition of the first plurality of ~~one or more~~
3 partitions has one or more objects of the plurality of
4 objects.

1 11. (Currently Amended) The method of claim 6, wherein

2 the interconnecting of objects substantially
3 independently is subject ~~at least~~ to boundary conditions of
4 the second plurality of partitions.

1 12. (Currently Amended) The method of claim 6, wherein
2 the interconnecting of objects substantially
3 independently is subject ~~at least~~ to a first partition of
4 the second plurality of partitions locking at least a net
5 shared by at least the first partition and a second
6 partition of the second plurality of partitions to prevent a
7 change of the net by the second partition of the second
8 plurality of partitions.

1 13. (Original) The method of claim 6, wherein
2 each partition of the first plurality of partitions is
3 represented by at least two partitions of the second
4 plurality of partitions.

1 14. (Currently Amended) The method of claim 6, wherein
2 each of the first level [[,]] and the second level of
3 the IC design includes the at least two metal routing
4 layers.

1 15. (Currently Amended) The method of claim 6, wherein

2 ~~each of~~ the first level ~~, and the second level~~ of the
3 IC design at least includes one layer of the at least two
4 metal routing layers, and
5 the second level of the IC design includes the at least
6 two metal routing layers.

1 16. (Currently Amended) A method of routing an
2 integrated circuit (IC) design, comprising:
3 accessing the IC design including a plurality of
4 objects having at least two metal routing ~~on one or more~~
5 layers;
6 accessing a first level for the IC design, wherein the
7 first level of the IC design is partitioned into a first
8 plurality of ~~one or more~~ partitions, and the plurality of
9 objects of the IC design are among the first plurality of
10 ~~one or more~~ partitions; and
11 forming a second level for the IC design, including:
12 partitioning the ~~[[second]]~~ first level into a
13 second plurality of partitions, wherein one or more
14 partitions of the first plurality of partitions is
15 represented by at least two partitions of the second
16 plurality of partitions;
17 allotting the second plurality of partitions among
18 a plurality of areas, such that each area of the

19 plurality of areas includes one or more partitions of
20 the second plurality of partitions; and
21 within each area of the plurality of areas,
22 interconnecting objects substantially independently of
23 other areas of the plurality of areas using the at
24 least two metal routing layers.

1 17. (Original) The method of claim 16, wherein
2 the routing is multithreaded at least at a first time.

1 18. (Original) The method of claim 16, wherein
2 the routing is single threaded at least at a first
3 time.

1 19. (Currently Amended) The method of claim 16,
2 wherein
3 one or more partitions of the first plurality of ~~one or~~
4 ~~more~~ partitions has no objects of the plurality of objects.

1 20. (Currently Amended) The method of claim 16,
2 wherein
3 every partition of the first plurality of ~~one or more~~
4 partitions has one or more objects of the plurality of
5 objects.

1 21. (Currently Amended) The method of claim 16,
2 wherein
3 the interconnecting of objects substantially
4 independently is subject ~~at least~~ to boundary conditions of
5 the second plurality of partitions.

1 22. (Currently Amended) The method of claim 16,
2 wherein
3 the interconnecting of objects substantially
4 independently is subject ~~at least~~ to boundary conditions of
5 the plurality of areas.

1 23. (Currently Amended) The method of claim 16,
2 wherein
3 the interconnecting of objects substantially
4 independently is subject ~~at least~~ to a first partition of
5 the second plurality of partitions locking at least a net
6 shared by at least the first partition and a second
7 partition of the second plurality of partitions to prevent a
8 change of the net by the second partition of the second
9 plurality of partitions.

1 24. (Currently Amended) The method of claim 16,
2 wherein

3 the interconnecting of objects substantially
4 independently is subject ~~at least~~ to a first area of the
5 plurality of areas locking at least a net shared by at least
6 the first area and a second area of the plurality of areas
7 to prevent a change of the net by the second area of the
8 plurality of areas.

1 25. (Currently Amended) The method of claim 16,
2 wherein
3 each of the first level [[,]] and the second level of
4 the IC design includes the at least two metal routing
5 layers.

1 26. (Currently Amended) The method of claim 16,
2 wherein
3 ~~each of the first level of the IC design , and the~~
4 ~~second level~~ at least includes one layer of the at least two
5 metal routing layers, and
6 the second level of the IC design includes the at least
7 two metal routing layers.

1 27-70. (Cancelled)

1 71. (New) The method of claim 6, wherein

2 the plurality of objects are cells of an IC cell
3 library.

1 72. (New) The method of claim 6, wherein
2 the interconnecting of objects is a graph based
3 routing.

1 73. (New) The method of claim 6, wherein
2 the interconnecting of objects is a combination of an
3 area based routing and a graph based routing.

1 73. (New) The method of claim 6, wherein
2 the interconnecting of objects within the second
3 plurality of partitions is a graph based routing,
4 the interconnecting of objects between the second
5 plurality of partitions is an area-based routing, and
6 the interconnecting of objects between the first
7 plurality of partitions is an area-based routing.

1 74. (New) The method of claim 6, further comprising:
2 prior to the interconnecting of objects in each
3 partition of the second plurality of partitions at the
4 second level,
5 forming a third level of the IC design, including

6 partitioning the second level of the IC design
7 into a third plurality of partitions, wherein one or
8 more partitions of the second plurality of partitions
9 is represented by at least two partitions of the third
10 plurality of partitions; and

11 within each partition of the third plurality of
12 partitions, interconnecting objects substantially
13 independently of other partitions of the third
14 plurality of partitions using the at least two metal
15 routing layers.

1 75. (New) The method of claim 74, further comprising:
2 after the interconnecting of objects in each partition
3 of the second plurality of partitions at the second level,

4 within each partition of the first plurality of
5 partitions at the first level, interconnecting objects
6 substantially independently of other partitions of the
7 first plurality of partitions using the at least two
8 metal routing layers.

1 76. (New) The method of claim 6, wherein
2 the at least two metal routing layers are an alloy.

1 77. (New) The method of claim 6, wherein

2 at least two partitions of the first plurality of
3 partitions have differing shapes or sizes.

1 78. (New) The method of claim 16, wherein
2 the plurality of objects are cells of an IC cell
3 library.

1 79. (New) The method of claim 16, wherein
2 the interconnecting of objects is an area-oriented
3 graph based routing by an area-oriented multi-threaded
4 graph-based detail router.

1 80. (New) The method of claim 16, wherein
2 the interconnecting of objects is a combination of a
3 grid based routing by a grid based router and a graph based
4 routing by a graph based router.

1 81. (New) The method of claim 16, wherein
2 the at least two metal routing layers are an alloy.

1 82. (New) The method of claim 16, wherein
2 at least two partitions of the first plurality of
3 partitions have differing shapes or sizes.

1 83. (New) A method of routing an integrated circuit
2 (IC) design, comprising:
3 parsing IC design information including a plurality of
4 cells of a cell library to support at least two metal wire
5 routing layers for the IC design;
6 receiving a design netlist to access a first level for
7 the IC design, wherein the first level of the IC design is
8 partitioned into a first plurality of partitions, and the
9 plurality of cells of the IC design are among the first
10 plurality of partitions;
11 generating a topological wiring between the first
12 plurality of partitions at the first level of the IC design
13 using at least one layer of the at least two metal wire
14 routing layers; and
15 forming a second level for the IC design, including
16 partitioning the first level of the IC design into
17 a second plurality of partitions, wherein each of the
18 first plurality of partitions is represented by at
19 least two partitions of the second plurality of
20 partitions,
21 generating a wiring between the second plurality
22 of partitions at the second level of the IC design
23 using at least one layer of the at least two metal wire
24 routing layers, and

25 generating a detailed wiring using a graph-based
26 routing within each of the second plurality of
27 partitions to interconnect the cells substantially
28 independently of other partitions of the second
29 plurality of partitions using the at least two metal
30 wire routing layers.

1 84. (New) The method of claim 83, wherein
2 the IC design information of the cells includes a
3 blockage within a first cell, and
4 the generating of the detailed wiring using the graph-
5 based routing is responsive to the blockage within the first
6 cell.

1 85. (New) The method of claim 83, wherein
2 the at least two metal wire routing layers are an
3 alloy.

1 86. (New) The method of claim 83, wherein
2 at least two partitions of the first plurality of
3 partitions have differing shapes or sizes.

1 87. (New) The method of claim 83, wherein

2 the topological wiring between the first plurality of
3 partitions at the first level of the IC design is generated
4 using an area based global routing.

1 88. (New) The method of claim 83, wherein
2 the topological wiring between the first plurality of
3 partitions at the first level of the IC design is generated
4 using a grid-based global routing.

1 89. (New) The method of claim 88, wherein
2 the wiring between the second plurality of partitions
3 at the second level of the IC design is generated using the
4 grid-based global routing.

1 90. (New) The method of claim 88, wherein
2 the wiring between the second plurality of partitions
3 at the second level of the IC design is generated using the
4 graph-based routing.